REMARKS

Claims 1-12 are pending of which claims 1 and 7 are independent. Claims 1, 2, 3, 5, 7, 9, 10 and 12 have been amended. It should be noted that several of the claims have been clarified by amendment above. Unless amended claim language is explicitly referred to below to distinguish over a document applied in an art rejection, the clarifying amendments are intended to be non-substantive in nature and should not be viewed as a narrowing of claim scope or a surrender of claimed subject matter. Claims 13 and 14 have been added without the introduction of new matter. Reconsideration in light of the following remarks is respectfully solicited.

Claim Objections

The Office Action points out problems with antecedent basis in an objection to claims 2, 3, 5, 7, 9, 10 and 12. Applicant agrees with the Examiner's suggestions to correct antecedent basis, and has amended the claims accordingly. Withdrawal of the objection is respectfully solicited.

Claim Rejections – 35 U.S.C. § 103

Claims 1-6 and 8-12 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Nagata et al., "Measurements and Analysis of Substrate Noise Waveform in Mixed Signal IC Environment" (hereinafter "Nagata") in view of U.S. Patent Application Publication No. 2002/0022951 to Heijningen et al. (hereinafter "Heijningen"), which has been newly-cited and applied as prior art. Applicant respectfully traverses this claim rejection.

Because method claim 1 and apparatus claim 8 are counterparts, for ease of discussion, remarks will refer to claim 1.

The Office Action maintains the same position with respect to Nagata as in the previous Office Action. As such, Applicant's position with respect to Nagata will not be repeated. However, both the Applicant and the Examiner appear to agree that Nagata does not disclose or suggest

"determining the waveform of the source current in the digital circuit from the analysis model," and "representing the digital circuit...as *a time-division group of parasitic capacitors* comprising *parasitic capacitors* each connected between a source line and a ground line to be charged at a specific timing...," as claim 1 recites.

Heinjningen relates to a method for determining noise generated from mixed-signal ICs, and alleges to overcome problems with conventional noise analyses which factor only certain aspects that contribute to noise generation. For example, by forming digital circuitry and analog circuitry on the same substrate, the digital circuitry injects noise on the substrate that affects analog circuitry. (See Heinjningen, ¶ 0009). Analysis of such noise generation is very complex, and typically involves assumptions which in turn lessen accuracy of the analysis. (See Heinjningen, ¶ 0010). It is alleged further that gate dependency cannot be accurately modeled and substrate noise from a power supply is not taken into account. (See Heinjningen, ¶ 0012-13).

Heinjningen alleges to overcome these issues with basically a two-part simulation. The first simulation includes "a one-time characterization of all digital standard cells to extract substrate current generation for every possible switching combination ...." (Heinjningen, ¶ 0099, lines 2-5). In fact, this "standard cell characterization is performed once for every technology." (Heinjningen, ¶ 0103, lines 7-8). Macro models created include detailed substrate models for each standard cell and generated switching noise and power waveforms for all possible combinations. These models are compiled into a single library in advance, e.g., by using a circuit simulator such as SPICE. (See Heinjningen, ¶ 0100, lines 1-8).

The second simulation is a "gate level simulation, e.g. a VHDL gate level simulation (with an extracted VHDL gate library), for each design to extract the switching events." (Heinjningen, ¶ 0099, lines 4-7). All switching events are recorded and collected in a switching file. (See

Heinjningen, ¶ 0101, lines 3-4). In other words, using a simulator, Heijningen alleges to obtain records of switching events of the gate and to calculate the waveform of the noise current. (See Heinjningen, ¶ 0127)

A macro model selected from the library created during the first simulations is combined with the switching event data for the second simulation. This combination is alleged to result in an equivalent substrate model for the entire digital circuit and is used to simulate the total generated noise. (See Heinjningen, ¶ 0102).

In the paragraph spanning pages 4 and 5 of the Office Action, it is alleged that Heijningen discloses or suggests "representing the digital circuit...as *a time-division group of parasitic capacitors* comprising *parasitic capacitors* ...," as claim 1 recites. Specifically, it is stated that "determining the power supply noise requires determining a capacitance contribution for each cell (i.e. capacitor group) independently (i.e. time division groups) ...." Applicant disagrees. The Examiner seems to be characterizing Heijningen as charging each cell or capacitor group, whereas each capacitor of the time-division capacitor group "is to be charged at a specific timing ...," as claim 1 recites. The Examiner's characterization of the reference does not correspond to that recited by claim 1.

Moreover, the description referenced by the Examiner concerns the determination of power supply noise induced in a substrate during the first simulation for generating macro models, as described above. For the Examiner's convenience, paragraph 119 has been reproduced below.

> To accurately simulate noise coupling from the power supply, the ringing effects should also be included in the macro model. This requires that the circuit capacitance Ccir between power and ground is extracted for each cell and added to the macro model. This extraction is performed by a small signal (AC) simulation of the digital gate without the substrate model.

It appears that the Examiner relies on the statement "circuit capacitance Ccir between power and ground is extracted for each cell and added to the macro model." However, this statement has

no correlation to "representing the digital circuit ... as *a time-division group of parasitic capacitors* comprising *parasitic capacitors* each ... to be charged at *a specific timing* ...," as claim 1 recites. Just because Heijningen suggests determining C cir for each cell in no way reads on a "a time-division group of parasitic capacitors." Moreover, a cell represents a group of gates, which may include substrate resistors and well capacitors. (See Heinjningen, ¶ 0078, lines 6-8, and ¶ 0088, lines 1-5; See Office Action, page 5, lines 1-2). Therefore, Heinjningen teaches charging a cell (including a group of capacitors), and incorporating the results in the macro model library, and then re-configuring the cell (including a group of capacitors) for a different switching combination (it represents the digital circuit differently), charging, and incorporating the results of that cell to the macro model library. (Heinjningen, ¶ 0099, lines 2-5). This way, all of the possible switching combinations of the digital circuit may be compiled in a single library. Still, any given representation of a digital circuit taken from this library does not represent "the digital circuit ... as *a time-division group of parasitic capacitors* comprising *parasitic capacitors* each ... to be charged at *a specific timing* ...," as claim 1 recites, or at least there is no disclosure of suggestion of such a representation.

In the paragraph spanning pages 4 and 5 of the Office Action, the Examiner appears to allege that Heinjningen discloses or suggests "determining the waveform of the source current in the digital circuit from the analysis model," as claim 1 recites. Specifically, the Examiner references paragraph 127 of Heijningen and alleges that "combining the individual waveforms to the determine the total noise waveform" is disclosed. While combining of such waveforms is disclosed, this disclosure in no way reads on that which is claimed. More particularly, claim 1 requires that the determination of the waveform of the source current in the digital circuit depends on the analysis model. Claim 1 further recites an analysis model in which the "time-division group of parasitic

capacitors" is connected in a certain manner. It follows that since Heijningen fails to disclose or suggest a time-division group of parasitic capacitors, it also fails to disclose an analysis model and determination of a waveform based on this group. Even the figures of Heijningen, show a group of capacitors. However, nowhere is it shown or described that this group may be a time-division group of parasitic capacitors.

Accordingly, Nagata in view of Heijningen fails to disclose or suggest each and every element of claim 1. Notwithstanding, the rejection does not establish a *prima facie* case of obviousness, as the initial burden has not been met. The supporting allegation motivation in the rejection is basically flawed. The first full paragraph on page 5 of the Office Action has been reproduced below in parts. Following each part is Applicant's response.

> It would have been obvious to one having ordinary skill in the art to modify the invention of Nagata to include determining the waveform of the source current in the digital circuit from the analysis mode and specifying that the parasitic capacitors be a time-series group of parasitic capacitors, as taught by Heijningen...

Applicant disagrees. As stated above, there is no disclosure or suggestion in Heijningen of a time-division group of parasitic capacitors.

> ... because Nagata does teach determining the noise as represented by voltage waveforms as well as that the capacitor groups are charged at specific timing according to the output of a truth table, as suggested by Heijningen...

Applicant disagrees. While Nagata may teach charging capacitors in accordance with a truth table, there is no disclosure of charging a time-division group of parasitic capacitors ... each capacitor ... at a specific timing, as claim 1 recites. Also, there is no suggestion in Heijningen that each capacitor is charged at specific timing according to the output of a truth table.. In fact, the above-quoted statement seems to be quite arbitrary. Nowhere in the detailed analysis provided in the Office Action is it stated or even suggested that Heijningen teaches charging at a specific timing according to a truth table.

> ... the combination would have provided a method for correctly determining the effect of capacitances (0088, lines 18-28), a simplified substrate and gate model based substrate voltage profile using a current profile (0089, lines 7-21), and a corresponding method for obtaining the power supply waveform by determining the effect of each group individually and then combining the waveforms of each group (0119 and 0127) in order to quickly and accurately determine the noise in a system having a large amount of gates ...

The Examiner is charged with the initial burden of providing the realistic requisite motivation for combining applied references to arrive at the claimed invention with a reasonable expectation of successfully achieving a specific benefit. *Smith Industries Medical System. v. Vital Signs*, 183 F.3d 137 (Fed. Cir. 1999). The Examiner's assertions of motivation correspond to very generalized statements in Heijningen concerning the advantages of the two part simulation for determining substrate noise characteristics. These statements in no way correspond to any specific benefit for modifying Nagata to include time-division group of parasitic capacitors. In fact, because the disclosures are so different, *i.e.,* Heijningen discloses determining capacitances for every possible switching configuration of a digital circuit whereas Nagata discloses representing a digital circuit as a group of capacitors, even if a specific benefit could be alleged, there is no possible reasonable expectation of success of achieving that benefit, at least not based on these two references.

Also, the fact that Heijningen discloses determining capacitances for every possible switching configuration of a digital circuit does not as a matter of fact make the combination obvious (especially considering there is basically no relationship between determining capacitances for every possible switching combination and representing a digital circuit as a time-division group of parasitic capacitors, as claim 1 recites).

The Examiner has not provided any reasonable showing in the prior art of a suggestion of the desirability to modify. The desirability to modify, "in order to quickly and accurately determine the noise in a system having a large amount of gates," amounts to desirability that is as

broad as, e.g., increasing circuit efficiency. In this case, it utterly lacks any factual support directed to the actual proposed combination. Such a broad and conclusory statement has been found to be an unrealistic requisite motivation for combining applied references.[1]

Also, because the Examiner has failed to provide any prior art suggestion for the modification of Nagata with a time-division group of parasitic capacitors, the basis of the rejection is no more than inappropriate hindsight reconstruction using Applicant's claim as a guide. *In re Warner*, 379 F.2d 1011 (CCPA 1967). The Examiner has not met the initial burden of providing realistic requisite motivation, thus rendering the obviousness rejection improper.

In the paragraph spanning pages 5 and 6 of the Office Action, the Examiner recites a portion of the background of the present application. There it is stated that generation of noise depends largely on change in source current. This is not disputed. However, then the Examiner states that "it would have been obvious ... that the source current waveform be determined from a source current waveform because the combination would have allowed for the analysis of the most likely representation of noises." It is not clear to what combination the Examiner refers. Claims 1-6 and 8-12 have been rejected as being obvious over the combination of Nagata and Heijningen, and not further in view of Applicants Admitted Prior Art (AAPA), as would be the case if the Examiner intended to cite the Background as prior art. If this is intended, the Examiner is required to reject the claims as being obvious over Nagata in view of Heijningen and further in view of AAPA to clarify the underlying rationale.

It is not clear what is meant by "that the source current waveform be determined from a source current waveform because the combination would have allowed for the analysis of the

[1] In *In re Lee*, 277 F.3d 1338 (Fed. Cir. 2002), the Federal Circuit held that purported motivation "to maximize the semiconductor device performance" lacks factual support. The motivation stated by the Examiner comports very closely to the analysis disapproved by the Federal Circuit as the statements lack factual support.

most likely representation of noises." It is basically stated that it is obvious to determine results from results. Further, it is not understood how the combination would have allowed for the "most likely representation of noises." There is no teaching of what makes a particular representation "most likely," and it is quite unclear what is meant by this statement.

Applicant submits that the motivation cited in the Office Action is not a realistic requisite motivation for combining applied references to arrive at the claimed invention with a reasonable expectation of successfully achieving a specific benefit. *Smith Industries Medical System. v. Vital Signs*, 183 F.3d 137 (Fed. Cir. 1999).

In accordance with the foregoing, the combination proposed in the latest rejection fails to disclose or suggest each and every element of claim 1 or claim 8, and further the detailed explanation does not satisfy the initial burden on the Patent Office to establish all elements of a *prima facie* case of obviousness. Claims depending there from are patentable based at least on dependency to claim 1 or 8, and for the reasons expressed above.

Claim 7 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagata in view of Heijningen and further in view of Mitra, previously cited. This rejection is respectfully traversed.

As claim 7 includes all the limitations set forth in claim 6, which in turn includes the limitations recited by claim 1, claim 7 is not obvious for the reasons discussed above. Withdrawal of the rejection is specifically solicited.

To the extent necessary, a petition for an extension of time under 37 C.F. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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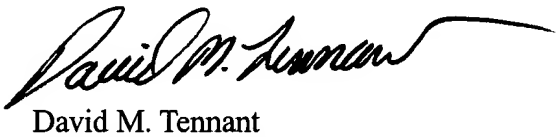

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